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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/482,332	01/14/2000	Michael A. Lamson	TI-28063	6840

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EXAMINER

FERRIS III, FRED O

ART UNIT PAPER NUMBER

2123

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/482,332

Applicant(s)

LAMSON ET AL.

Examiner

Fred Ferris

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 January 2002.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)                      4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)                      5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_                      6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. *Claims 1-31 have been presented for examination. Claims 1-31 have been rejected by the examiner.*

### ***Drawings***

2. *The drawings filed on 14 January 2000 have been approved by the examiner pending review by the draftsman.*

### ***Priority***

3. *Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. However, the provisional application upon which priority is claimed fails to provide adequate support under 35 U.S.C. 112 for claims 1-31 of this application. (Please see 112(1) rejection below.)*

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. ***Claims 1-31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in***

*the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.*

*Specifically, the **analysis generator** portion of the claimed invention has not been sufficiently disclosed in the specification. While the specification states that the model data analysis executes a “plurality of electrical calculation programs” (page 13, line 4), and that the “programs have been developed by the University of Arizona at Tucson” (page 13, line 13) no algorithm or techniques are provided that teach how one would implement the “plurality of electrical calculation programs” to “create the electrical analysis output file” as referenced in the independent claims. Further, merely stating that the programs “include two-dimensional and three-dimensional electrical analysis programs for capacitance as well as inductance” (page 13, line 15) does not provided enablement such that one skilled in the art would not know how to make and/or use the invention without undue experimentation.*

### **Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

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1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
5. ***Claims 1-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,455,775 issued to Huber et al in view of "Time-Domain Characterization of Packaging Effects via Segmentation Technique", M. Righi, IEEE Transactions on Microwave Theory and Techniques, vol. 45, No. 10, October 1997.***

*While the specification for the claimed invention is delinquent in the areas cited above under 112(1) rejections, the examiner has made prior art rejections based on the limited scope of information contained in the specification.*

*Independent claims 1, 12 and 22 are drawn to:*

System, Computer implemented method and system for **modeling electronic structure** including:

**Input data generator**- characteristics of structure in segments, subdivisions, and compositions

**Segmentation generator**- select, organize, store, and convert segment files

**Analysis generator**- analyze converted segment file, create analysis output files from calculation sequence

**Integrator**- integrates analysis output files in sequence into model file store in report storage

**Output generator**- creates summary files in specific format

*Regarding independent claims 1, 12, and 22: Huber discloses a computer system for designing physical packages for electronic components (structures) that includes an **input system** (Input Data Generator) for inputting physical design characteristics (Fig. 2, CL4-L38, CL5-L4), an **analysis program** (analysis generator) for*

*analyzing and assigning various characteristics of the design* (CL2-L55, CL6-L4), and a **partitioning program** (segmentation generator) for partitioning portions an integrated circuit, physical areas of a chip, chip carriers, boards, or card. (CL2-L44, CL11-L18, CL12-L27, Figs. 3 and 9) (Also see, Abstract, Summary of Invention, CL5-L4-14, Figs. 1, 6-8) The various “generators” of the claimed invention are disclosed to be software modules capable of performing a particular function (i.e. segmentation, analysis, input/output etc.) and appear to make use of features (i.e. file conversion, formats, etc.) which are inherent in the referenced commercially available software packages such as Pro/Engineer, SPICE, AutoCAD, etc. and, hence, would have been an obvious choice for use in designing a system for modeling an electronic structure.

*Huber discloses partitioning of circuit elements, but does not explicitly teach segmentation of conductors in an electronic structure.*

*Righi discloses geometric segmentation of package conductors where the structure is divided into multiple segments (subdivisions) in order to analyze the circuit behavior. (Abstract, Section II – TLM Analysis, Section III – Segmentation, Figs. 7, 10, 11) Organizing and converting segment files would be obvious and necessary since the claimed invention uses standard formats, i.e. SPICE, DXF, IGES, etc.*

*It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teaching of Huber relating to a computer system for designing physical packages for electronic components (structures), with the teachings of Righi relating to the geometric segmentation of package conductors where the structure is divided into multiple segments (subdivisions) to realize the claimed*

*invention. An obvious motivation exists since, as referenced in the prior art, segmentation of circuit elements improves the prediction of the performance of a packaged circuit at a fraction of the computational cost. (Righi, pp. 1901)*

Regarding dependent claims 2-11, 13-21, and 23-31: As cited above Righi teaches **segmentation** arrangement and **modeling** of a semiconductor **device** in an **integrated circuit package** (leadframe) containing a **substrate** and **conductive pattern** and further considers **geometry, frequency, resistances, capacitances, and inductances** of the conductive pattern. (Figs. 7-10, Section II A-C, Section III)

### **Conclusion**

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 5,629,861 issued to Kim teaches electronic package design.

U.S. Patent 6,022,649 issued to Neoh et al teaches structures of segments and sub-segments.

"New Electrical Modeling Approach for Simultaneous Switching Noise for High-Performance Packages", K. Kato, 1996 Electronic Components and Technology Conference, pp. 739-746, IEEE 1996 teaches segmentation in electronic packages.

*Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday.*

*Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.*

The Official Fax Numbers are:

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Official	(703) 746-7239
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